A CMOS Image Sensor with Nearly Unity-Gain Source Follower and Optimized Column Amplifier

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***Abstract*—This paper presents a CMOS image sensor with in-pixel nearly unity-gain pMOS transistor based source followers and optimized column-parallel amplifiers. The prototype sensor has been fabricated in a 0.18 µm CMOS process. By eliminating the body effect of the source follower transistor, the voltage gain for the pixel-level readout circuitry approaches unity. The use of a single-ended common-source cascode amplifier with ground rail regulation improves the PSRR of the column-parallel analog front-end circuitry and further the noise performance. Electrical characterization results show that the proposed pixel improves the conversion gain after the in-pixel source follower by 42% compared to that of the conventional structure. The prototype sensor with proposed readout architecture reaches a 1.1e$^-$ input-referred temporal noise with a column-level ×16 analog gain.**

Keywords—CMOS image sensor; source follower; amplifier; regulator; noise;

I. INTRODUCTION

The imaging quality of CMOS image sensors (CIS) at low light levels is highly susceptible to noise originating from a variety of sources along the signal readout chain [1]. The low frequency noise, i.e. random telegraph signal (RTS) noise and flicker noise generating by the in-pixel source follower (SF) has been recognized as one of the most significant noise contributor. Implementing a SF with a pMOS transistor can provide substantial low frequency noise reduction and has been investigated in a few recent works [2-5]. However, this approach also suffers from the voltage gain degradation due to the higher body effect trans-conductance of pMOS transistors, which increases the noise contribution of succeeding circuits when referred to the input of the source follower. Another dominant noise source in the CIS is located at the column amplifier. Besides its intrinsic noise generated by transistors, the interference noise coming from the supply and ground lines due to the existence of the co-integrated digital processing circuits also plays a role impacting the noise performance of the CIS.

In this work, a prototype image sensor targeted for low noise applications is presented. In view of the advantage of the pMOS transistor over its nMOS counterpart in minimizing the low frequency noise, we propose to investigate how a pMOS SF without body effect can further reduce the input-referred noise in the CIS. Moreover, in order to improve the power-supply-rejection-ratio (PSRR) of the column readout circuits and hence their noise performance, a single-ended cascode common source amplifier with local ground line regulation has been adopted as the operational trans-conductance amplifier (OTA) in the column level [6].

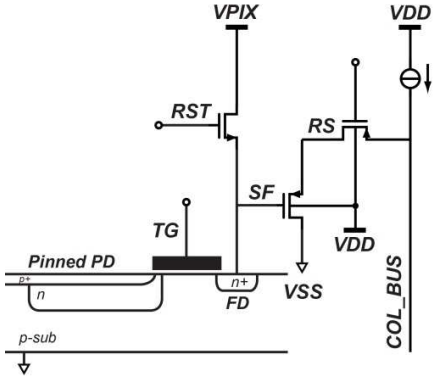

Fig. 1. Schematic of a pMOS-based SF pixel structure with body effect.

II. SENSOR ARCHITECTURE

A. Pixel Structure

One of the pixel structures dedicated for low-noise CMOS image sensors is to utilize a pMOS transistor as the SF in combination with a standard n-type PPD, as shown in Fig.1. In order to maintain the source-body junction reverse biased, the bulk terminal of the pMOS-based SF is conventionally connected to the supply voltage, sharing a common n-well with other pMOS transistors (RST, RS) in the same pixel, which results in the body effect. MOS body effect trans-conductance g_{mb} refers to the change in the drain current by a change in body-source voltage V_{BS} with all other terminals held at a constant voltage. It appears between the drain and source terminals, as a gain factor for the V_{BS} controlled current source in the MOS small-signal model [7]. Also in small-signal analysis, the body effect trans-conductance g_{mb} is often expressed as a fraction of the gate trans-conductance g_m. According to [7], the ratio $\eta = g_{mb}/g_m$ increases with a higher substrate doping concentration and a lower presence body-source voltage. Assuming the output resistance of both the current source and the SF are infinite, the voltage gain (A_v) of the source follower approaches $g_m/(g_m+g_{mb}) = 1/(1+\eta)$. Given the fact that the body-source potential V_{BS} for pMOS SF is much lower than that of the nMOS SF, which is typically a couple of mV, whereas above 1V for nMOS. The in-pixel

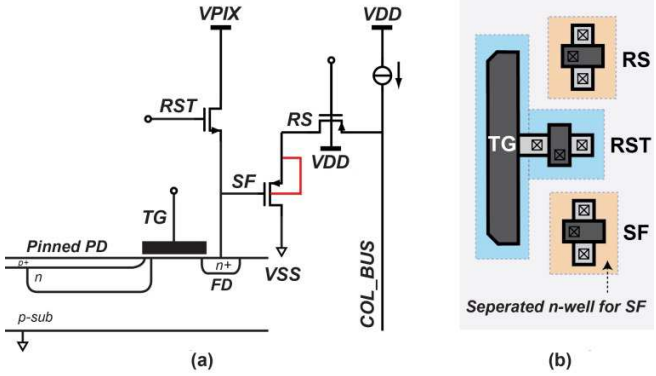

Fig. 2. Schematic of a pMOS-based SF pixel structure without body effect and the corresponding in-pixel transistors layout.

pMOS SF suffers from a more pronounced body effect and hence results a less-than-unity voltage gain, which ranges from 0.6 to 0.7 depending on the input level.

As shown in Fig.2, an effective approach to eliminate this undesirable body effect of an in-pixel SF is to employ a separated n-well for the SF transistor instead of sharing the common n-well with other in-pixel transistors [8]. Benefiting from this separation, the bulk terminal of the SF can be directly tied to the source terminal. Thus, the contribution of g_{mb} to the overall output trans-conductance of the SF could be ignored. As such, the voltage gain of a pMOS SF without body effect approaches unity. The simulation results show that the proposed SF structure achieves a -95mdB (0.988) voltage gain, which is nearly unity.

B. Column Amplifier Structure

Following the pixel-level SF readout structure, the CIS front-end signal conditioning in each column is performed by a switched-capacitor CDS amplifier, as shown in Fig.3. In order to achieve an input-referred noise level that is small enough compared to the pixel's output noise, an improved common-source cascode amplifier has been used as the OTA for the column amplifier.

A conventional common-source cascode stage is inherently single-ended and senses the voltage difference between the input node and the ground rail. Accordingly, any noise that appears on the ground rail will also be manifest at the output node. To address this problem, we propose to locally generate a ground rail with a column-level low-dropout (LDO) regulator for each column amplifier, so as to reject interference from the common ground. Due to the fact that the loading currents for this column-level LDO regulator are known and approximately constant, the scheme implementation of this regulator can be kept simple to fit the column pitch. A single-transistor-controlled (STC) LDO based on a flipped voltage follower [9] is adopted as the topology for the regulator as shown in Fig.4. When V_{OUT_REG} varies, M_C provides an error voltage at its drain, so as to control the drain current delivered by M_P and to regulate V_{OUT_REG}. With this control, the STC LDO is capable of providing sufficient loop gain and hence provides a PSRR to

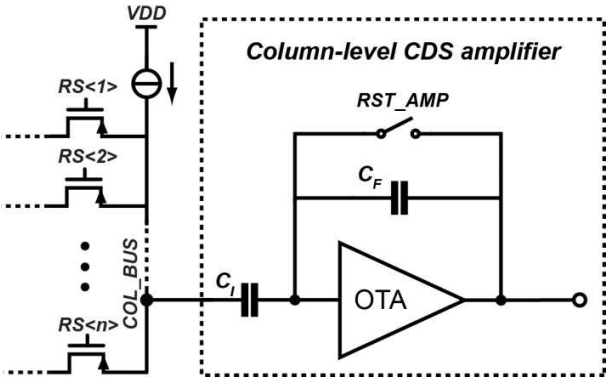

Fig. 3. The column-parallel amplifier with CDS function.

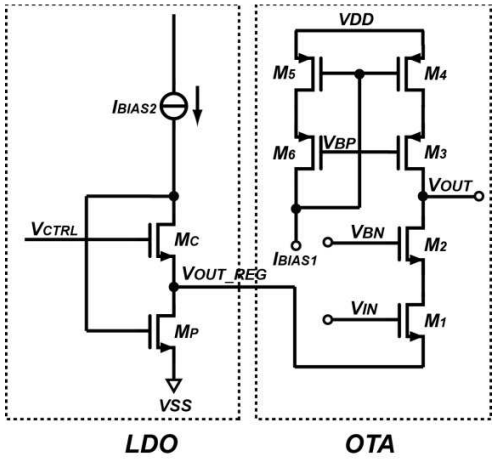

Fig. 4. Common source cascode amplifier with local ground-rail regulator.

ground better than -38dB within the frequency range of interest according to the simulated results.

C. Implementation Details

To evaluate the proposed noise reduction techniques, a CIS pixel array has been divided into two sub-arrays, one of which is implemented with the conventional pMOS-based SF structure with body effect as the reference pixel, and the other with the proposed SF structure without body effect. Each sub-array contains 32(H) × 64(V) pixels and features the same pixel pitch of 11µm. Moreover, the size of the floating diffusion (FD) node and the studied SF transistors for both pixel sub arrays are identical in the layout.

The column-level switched-capacitor amplifier are placed at the bottom of the pixel array with 11µm pitch. To enhance the dynamic range of the column amplifier, a programmable gain function is implemented by including switchable input and feedback capacitors. Five gain levels (×1, ×2, ×4, ×8, ×16) are provided, among which the ×16 gain step is designed to achieve the highest sensitivity and the best noise performance.

III. Experiment Results

The test sensor with the proposed readout architecture has been fabricated in a 0.18µm CIS process technology. Fig.4 presents a micro-photograph of the prototype chip.

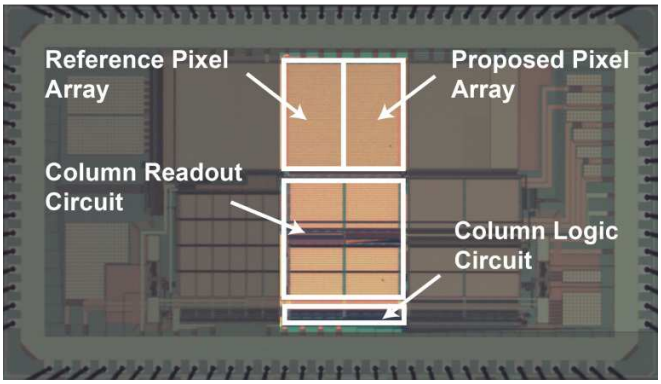

Fig. 5. Photograph of the prototype sensor.

Fig. 6 shows the measured plot of the noise variance as a function of the average output signal voltage value for both pixels. The conversion gain (CG) after the source follower for the reference pixel with body effect is 71μV/e^-, while for the proposed pixel without body effect is 122μV/e^-. As the measured resultant CG is not only determined by the FD capacitance but also is associated to the voltage gain of the source follower. The proposed SF structure improves the conversion gain after the in-pixel SF by 42% compared to the reference pixel.

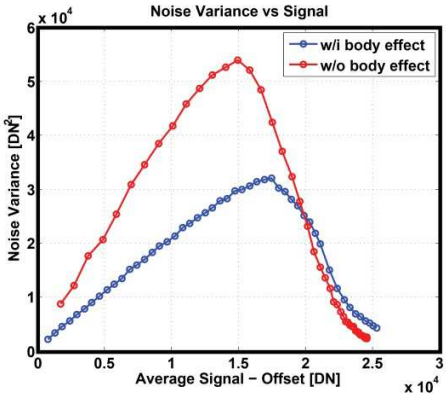

Fig. 6. Conversion gain for pMOS source follower w/i and w/o body effect.

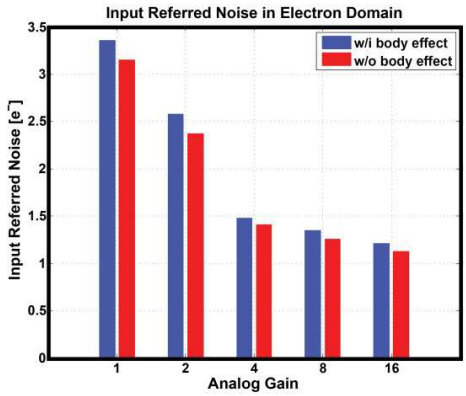

Fig. 7. Input-referred noise vs. column amplifier gain.

Temporal noise characterization has been done in dark and implemented by using the reset voltage as an input for the SF and keeping the transfer gate TG and the reset gate RST off during the measurement period. During the measurement, only correlated double sampling (CDS) was implemented. The RMS temporal noise is first measured by a board-level 16bit ADC and then referred to the electron domain by dividing it with the measured conversion gain. Fig.7 shows the input-referred noise voltage for proposed pixels as a function of the column-parallel amplifier gain. For the gain steps of 1 and 2, the proposed pixel structure improves the input-referred noise by 10%. As the gain step of the column amplifier increases, the difference of the noise levels between the two types of pixels becomes smaller, which indicates that the effectiveness of succeeding noise reduction by the high gain of the column amplifier becomes dominant. By adopting the proposed pixel structure and amplifier configuration, the prototype CIS features an input-referred noise of 1.1e^- with a column-level ×16 analog gain.

IV. Conclution

A CMOS image sensor targeted for low noise applications has been presented. It adopts various techniques both at pixel level and column level, including in-pixel nearly unity gain pMOS-based source followers and improved column-parallel amplifiers. By connecting the body terminal to the source, the loss of voltage gain from unity has been avoided for the in-pixel source follower. A single-ended cascode amplifier with ground-rail regulation is employed to achieve a better PSRR to ground. The prototype sensor with proposed readout architecture reaches a 1.1e^- input-referred temporal noise with a column-level ×16 analog gain.

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